As microprocessors grow more powerful and complex, engineers dream of putting an entire computer system on a single chip. Such chips would be smaller, faster, and more energy efficient than today’s designs. To get there, though, we will need to reinvent how we design chips, Associate Professor Luca Carloni argues.

Today, engineers create microprocessors using tools that help them build circuits from libraries of proven designs. Yet new technologies pose many problems for traditional tools. In the past, for example, chips synchronized all operations with a single clock. “Compared to the times needed for computation, on-chip communication was basically instantaneous,” Carloni explained. “Today, local calculations run so fast, it takes several clock cycles for remote signals to arrive. This is a physical issue we need to address.”

Carloni ticks off other problems. New chips have multiple processors, or cores, whose parallel operations create new challenges in programmability. Billions of transistors create new levels of complexity and generate lots of heat that is hard to remove. Resolving these issues has extended the amount of time and design iterations needed to create new chips.

Those same emerging technologies also offer new opportunities. Instead of trying to develop a system-on-chip with old tools, Carloni proposes reinventing chip architectures and the tools used to design them. “We need to create communication infrastructures that make it easier to integrate new components into our designs,” he said.

His solution is a network on a chip. “Our vision is to create an on-chip communication and control infrastructure. When we have a network that touches every component on a chip, we can dynamically configure the processor to optimize speed or efficiency. We don’t have the solution yet, but we’re working on it.”

He envisions a collection of communications elements – nanoscale wires, switches, and routers – to move data around the chip. The cores would have standard interfaces to plug into the network. A new generation of tools would support component selection and network optimization.

“Instead of designing links between each circuit, you would plug components into a standardized backbone,” Carloni said. “This makes it much easier to design processors. Engineers could continuously upgrade and test new components, then plug them in and know they would work on the chip.”

Networked chips would also support multiple cores running at different clock rates. Chips could assign tasks to different cores to optimize speed or reduce energy use. “The path towards green computing systems starts with more efficient communication infrastructures,” Carloni said.

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Networking Chips

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